What is claimed is:

1. A method for manufacturing a semiconductor device, comprising:

forming an impurity precipitation region by introducing an impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, and

performing high selectivity anisotropic etching of the material substrate or the material layer with the impurity precipitation region used as a micro mask to form a conic body the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer.

2. A method for manufacturing a semiconductor device according to claim 1, wherein:

the impurity precipitation region has an etching rate different from that of a main component material of the semiconducting material substrate or the semiconducting material layer, and

the impurity precipitation region is formed by thermally treating the impurity introduced into the predetermined position of the semiconducting material substrate or the semiconducting material layer to precipitate into a crystal of the semiconducting material substrate or the semiconducting material layer.

3. A method for manufacturing a semiconductor device according to claim 1, wherein a material for the semiconducting

material substrate or the semiconducting material layer is silicon, and the impurity to be introduced is oxygen.

4. A method for manufacturing a semiconductor device according to claim 1, wherein the semiconducting material substrate or the semiconducting material layer further contains a second impurity which is bonded to the introduced impurity easier than to the material element of the semiconducting material substrate or the semiconductive material layer.

5. A method for manufacturing a semiconductor device according to claim 4, wherein:

a material for the semiconducting material substrate or the semiconducting material layer is silicon,

the introduced impurity is oxygen, and

the second impurity is boron.

6. A method for manufacturing a semiconductor device according to claim 1, wherein the process of forming the impurity precipitation region as the micro mask comprise:

forming an ion implantation mask, which is open at a target conic body forming region and covers the region other than the target region, on the surface of the semiconducting material substrate or the semiconducting material layer,

performing ion implantation of the impurity into the semiconducting material substrate or the semiconducting material layer, and

thermally treating the implanted impurity to precipitate

it into the crystal of the material substrate or the material layer.

7. A method for manufacturing a semiconductor device according to claim 1, wherein the process of forming the impurity precipitation region as the micro mask comprises:

growing the semiconducting material substrate or the semiconducting material layer by an epitaxial method in a direction of a target conic body forming height,

adding gas containing the impurity to a material gas at a target micro mask forming height to further grow the semiconducting material substrate or the semiconducting material layer by the epitaxial method, and

removing an epitaxial growth layer containing the impurity excepting the target conic body forming region.

8. A method for manufacturing a semiconductor device, comprising:

forming an impurity precipitation region by introducing an impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer,

performing high selectivity anisotropic etching of the material substrate or the material layer with the impurity precipitation region used as a micro mask to form a truncated conic body the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer, and

exposing the top surface of the formed truncated conic

body by etching and performing high selectivity anisotropic etching of the leading end of the truncated conic body in the shape of a mortar from the top surface to the bottom of the truncated body to form the truncated conic body having an annular leading end.

9. A method for manufacturing a semiconductor device, comprising:

forming an impurity precipitation region by introducing an impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer,

performing high selectivity anisotropic etching of the material substrate or the material layer with the impurity precipitation region used as a micro mask to form a conic body the top of which is the micro mask on an etching exposure surface of the material substrate or the material layer,

forming an embedding layer on the etching exposure surface so to embed the conic body,

etching the embedding layer so to etch the top of the embedded conic body, and

performing high selectivity anisotropic etching of the top surface of the conic body exposed to the surface into the shape of a mortar extending toward the bottom of the conic body to form the truncated conic body having an annular leading end.

10. A semiconductor device, comprising a conic body formed on a semiconducting material substrate or a semiconducting material layer, the conic body having a radius of curvature of several to

ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

11. A semiconductor device, comprising a truncated conic body formed on a semiconducting material substrate or a semiconducting material layer, the truncated conic body having a radius of curvature of several to ten or more nm in the vicinity of its leading end or a diameter of about several to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more, and an annular shape at its leading end with the center of the top surface partly removed.

12. A semiconductor device according to claim 11, wherein the truncated conic body has its leading end removed in the shape of a mortar from the top face toward the bottom of the truncated conic body to form the annular shape at the leading end.

13. A single electron semiconductor device for controlling propagation of a single or a small number of electrons, comprising a silicon needle conic body protruded on a substrate as at least a part of a propagation passage for the single or the small number of electrons.

14. A device according to claim 13, further comprising:

a source region and a drain region closely disposed on the side of the silicon needle conic body with the silicon needle conic body intervened therebetween,

wherein the silicon needle conic body is used as a quantum dot, and between the silicon needle conic body and the source region, between the silicon needle conic body and the drain region, between the source and drain regions, and a space between the silicon needle conic bodies where the silicon needle conic body is formed in multiple numbers is used as a small tunnel junction to control the propagation of a single or a small number of electrons between the source region and the drain region.

15. A single electron semiconductor device according to claim 13, further comprising:

a potential control electrode for controlling the potential in the conic body disposed around the side face of the silicon needle conic body,

wherein the propagation of a single or a small number of electrons is controlled between the vicinity of the bottom and the vicinity of the leading end of the silicon needle conic body by the potential control by the potential control electrode.

16. A single electron semiconductor device according to claim 13, further comprising:

a potential control electrode for controlling the potential in the conic body disposed around the side face of the silicon needle conic body,

wherein the vicinity of the side face of the silicon needle conic body is depleted by the potential control by the potential control electrode to form a quantum wire region at the

core of the silicon needle conic body.

17. A device according to claim 16, wherein the silicon needle conic body has a conic shape with a radius of curvature of several nm to ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

18. A device according to claim 16, wherein:

the silicon needle conic body has a truncated conic body with a radius of curvature of several nm to ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more, and

the leading end of the truncated conic body has an annular shape with its center partly removed.

19. A single electron semiconductor device for controlling propagation of a single or a small number of electrons, comprising:

a silicon needle conic body protruded on a substrate, and

a conducting material layer formed on the substrate so to bury at least the lower portions of the silicon needle conic bodies, wherein:

peripheral regions of the silicon needle conic bodies of the conducting material layer are functioned as quantum dots and small tunnel junctions to control the propagation of a single or a small number of electrons in the plane direction of the

conducting material layer.

20. A single electron semiconductor device according to claim 19, wherein:

the silicon needle conic body is closely formed in multiple numbers so to be arranged in a breadth direction of the conducting material layer, and

the conducting material layer in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot and the minute channel.

21. A single electron semiconductor device according to claim 19, wherein:

the silicon needle conic body is closely formed in multiple numbers in a direction along the end of the conducting material layer,

the conducting material layer in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot, and

the conducting material layer in a region intervened between the plurality of arranged silicon needle conic bodies and the end of the conducting material layer functions as the small tunnel junction.

22. A single electron semiconductor device according to claim 19, wherein:

the silicon needle conic body is closely formed in multiple numbers in a direction along the end of the conducting

material layer,

a depletion layer is formed in the conducting material layer in the peripheral region having the silicon needle conic body at the center, and

a quantum dot and a small tunnel junction are formed in a region between the depletion layer end in the conducting material layer and the end of the conducting material layer.

23. A device according to claim 19, wherein the silicon needle conic body has a radius of curvature of several nm to ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

24. A device according to claim 19, wherein:

the silicon needle conic body has a truncated conic body with a radius of curvature of several nm to ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more, and

the leading end of the truncated conic body has an annular shape with its center partly removed.

25. A semiconductor memory for storing information by accumulating electric charges in a capacitor configuring each memory unit, comprising:

a needle of silicon crystal formed in each memory unit, and a capacitor having the side face of the needle as one of

electrodes.

26. A semiconductor memory according to claim 25, wherein a switching transistor is formed on a part of the silicon crystal needle to supply the capacitor with electric charges.

27. A semiconductor memory according to claim 26, wherein the switching transistor is formed at the base of the silicon crystal needle, and the capacitor is formed at the leading end.

28. A semiconductor memory according to claim 26, wherein the switching transistor is formed at the leading end of the silicon crystal needle, and the capacitor is formed below the switching transistor.

29. A device according to claim 25, wherein the silicon crystal needle has a conic shape with a radius of curvature of several nm to ten or more nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

30. A method for manufacturing a single electron semiconductor device for controlling propagation of a single or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

performing high selectivity anisotropic etching of the silicon substrate or the silicon layer with the impurity

precipitation region used as a micro mask to form a silicon needle conic body the top of which is the micro mask, and

using the silicon needle conic body as at least a part of a propagation route of the single or the small number of electrons of the single electron semiconductor device.

31. A method for manufacturing a single electron semiconductor device for controlling propagation of a single or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

performing high-selectivity anisotropic etching of the silicon substrate or the silicon layer with the impurity precipitation region used as a micro mask to form a silicon needle conic body on the substrate the top of which is the micro mask,

forming a conducting material layer on the substrate so to bury the silicon needle conic body and at least a lower portion of the silicon needle conic body, and

functioning the peripheral region of the silicon needle conic body of the conducting material layer as a quantum dot and a small tunnel junction to control the propagation of a single or a small number of electrons in the planar direction of the conducting material layer.

32. A semiconductor memory for storing information, comprising:

an impurity precipitation region in a single-crystal

silicon substrate or a single-crystal silicon layer,

a silicon crystal needle conic body formed in each memory unit on the substrate by subjecting the silicon substrate or the silicon layer to high selectivity anisotropic etching with the impurity precipitation region used as a micro mask, the silicon precipitation region having the micro mask at the top, and

a capacitor having the side face of the silicon crystal needle as one of electrodes,

wherein information is stored by accumulating electric charges into the capacitor.